IN THE CLAIMS

The following is a complete listing of the claims:

1. (currently amended) A Schmitt trigger configured to receive an input voltage and produce at an output node an output voltage that changes states with respect to a high voltage threshold and a low voltage threshold, comprising:

a first feedback path having a first transistor with a gate terminal coupled to the output node and with a second terminal coupled to the ground node to determine one of the voltage thresholds;

a second feedback path having a second transistor with a gate terminal coupled to the output node and with a second terminal coupled to the power supply voltage node to determine a remaining one of the voltage thresholds; and

at least one diode coupled to a path selected from the first feedback path and the second feedback path such that an on-current through the ~~first~~ selected ~~feedback~~ path is reduced as a supply voltage for the Schmitt trigger is reduced.

2. (original) The Schmitt trigger of claim 1, wherein the Schmitt trigger is a CMOS Schmitt trigger.

3. (currently amended) The Schmitt trigger of claim 1, wherein the selected path is the first feedback path ~~is configured to determine the low voltage threshold, the Schmitt trigger further comprising: a second feedback path configured to determine the high voltage threshold~~.

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4. (currently amended) The Schmitt trigger of claim 3, wherein the ~~first feedback path comprises a~~ first ~~PMOS~~ transistor comprises a first PMOS transistor having ~~a~~ its second

terminal coupled to the at least one diode and wherein the second ~~feedback path~~ transistor comprises a first NMOS transistor.

5. (original) The Schmitt trigger of claim 4, wherein the at least one diode comprises a first diode and a second diode.

6. (currently amended) The Schmitt trigger of claim 4, wherein the second terminal of the first PMOS transistor is a drain terminal, the at least one diode coupled between the drain terminal and the ~~a~~ ground node.

7. (currently amended) The Schmitt trigger of claim 1, wherein the selected ~~first~~ path is the second feedback path ~~determines the high voltage threshold, the Schmitt trigger further comprising: a second feedback path that determines the low voltage threshold~~.

8. (currently amended) The Schmitt trigger of claim 7, wherein the second ~~feedback path~~ transistor comprises a first NMOS transistor having ~~a~~ its second terminal coupled to the at least one diode and wherein the ~~second~~ first ~~feedback path~~ transistor comprises a first PMOS transistor.

9. (original) The Schmitt trigger of claim 8, wherein the at least one diode comprises a first diode and a second diode.

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10. (currently amended) The Schmitt trigger of claim 8, wherein the second terminal of the first NMOS transistor is a drain terminal, the at least one diode coupled between the drain

terminal and ~~a~~ the power supply voltage node ~~terminal~~.

11. (currently amended) The Schmitt trigger of claim 4, further comprising a second and a third PMOS transistor and a second and a third NMOS transistor all coupled in series between the ~~a~~ power supply voltage ~~terminal~~ node and the ~~a~~ ground node ~~terminal~~.

12. (original) A method of altering the hysteresis for a Schmitt trigger, the hysteresis being defined with respect to a high voltage threshold and a low voltage threshold, the Schmitt trigger including a first feedback path that determines one of the voltage thresholds, the method comprising:

changing a supply voltage for the Schmitt trigger; and

in response to the changed supply voltage, affecting an on-current through the first feedback path using at least one diode such that the determined voltage threshold satisfies a predetermined threshold.

13. (original) The method of claim 12, wherein the first feedback path determines the low voltage threshold, the adjusting the supply voltage act comprises lowering the supply voltage, and the affecting the on-current comprises reducing the on-current through the first feedback path such that the low voltage threshold is offset from ground by the predetermined threshold.

14. (original) The method of claim 12, wherein the first feedback path determines the high voltage threshold, the adjusting the supply voltage act comprises increasing the supply voltage, and the affecting the on-current comprises increasing the on-current through the first feedback path such that the high voltage threshold is offset from the supply voltage by the predetermined threshold.

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15. (original) A Schmitt trigger configured to receive an input voltage and produce at an output node an output voltage that changes states with respect to a high voltage threshold and a low voltage threshold, comprising:

a first feedback path having a first transistor with a gate terminal coupled to the output node and with a second terminal coupled to the ground node to determine one of the voltage thresholds;

a second feedback path having a second transistor with a gate terminal coupled to the output node and with a second terminal coupled to the power supply voltage node to determine a remaining one of the voltage thresholds; and

means for reducing an on-current through a path selected from the first feedback path and the second feedback path as a supply voltage for the Schmitt trigger is reduced.

16. (currently amended) The Schmitt trigger of claim 15, wherein the ~~first feedback~~ selected path ~~comprises a first PMOS transistor~~ is the second feedback path and the means for reducing the on-current comprises at least one diode.

17. (original) The Schmitt trigger of claim 16, wherein the at least one diode comprises a diode-connected PMOS transistor.

18. (original) The Schmitt trigger of claim 17, wherein the diode-connected PMOS transistor couples between ~~a~~ the ~~ground~~ power supply voltage node and ~~a drain~~ the second terminal of the first ~~PMOS~~ transistor.

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19. (cancelled)

20. (currently amended) The Schmitt trigger of claim 18 ~~19~~, further comprising:

a first inverter configured to invert the input voltage to provide an inverted output at an output terminal; and

a second inverter configured to invert the inverted output from the output terminal of the first inverter, wherein a drain of the first PMOS transistor couples to the output terminal of the first inverter.

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